AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (original) A semiconductor device comprising:

a memory unit having a plurality of addresses for temporarily storing a data signal;

a data signal providing unit for providing said data signal to said memory unit;

a driving unit for generating a control signal for controlling a functional element based on said data signal read out from said memory unit and providing said control signal to said functional element; and

a data-update control unit for successively providing an identical data signal over a plurality of times from an identical address in said memory unit.

2. (original) The semiconductor device as set forth in Claim 1,wherein said data-update control unit causes said data signal providing unit to suspend the operation of providing a data signal, in order to keep said data signal stored in said memory unit from being updated when successively providing the identical data signal to said functional element.

3. (original) The semiconductor device as set forth in Claim 1, wherein said data-update control unit causes said data signal providing unit to shut off a data signal transmission route from said data signal providing unit to said memory unit, in order to keep said data signal stored in said memory unit from being updated when successively providing the identical data signal to said functional element.

4. (original) A semiconductor device comprising:

a memory unit having a plurality of addresses for temporarily storing a data signal;

a driving unit for selecting a control signal input from outside for controlling a functional element based on said data signal read out from said memory unit and providing said control signal to said functional element; and

a data-update control unit for successively providing an identical signal over a plurality of times from an identical address in said memory unit.

5. (original) A semiconductor device comprising:

a memory unit having a plurality of addresses for temporarily storing a data signal;

a first driving unit for outputting to a functional element a signal for selecting, based on said data signal read out from said memory unit, a control signal input from outside for controlling said functional element;

a second driving unit for providing said control signal to said functional element; and

a data-update control unit for successively providing an identical signal over a plurality of times from an identical address in said memory unit.

6. (original) The semiconductor device as set forth in Claim 1, wherein said driving unit and said memory unit constitute a combined unit.

7. (original) The semiconductor device as set forth in Claim 4, wherein said driving unit and said memory unit constitute a combined unit.

8. (original) The semiconductor device as set forth in Claim 5, wherein said driving unit and said memory unit constitute a combined unit.

9. (original) The semiconductor device as set forth in Claim 1, wherein said driving unit, said functional element and said memory unit constitute a combined unit.

10. (original) The semiconductor device as set forth in Claim 4, wherein said driving unit, said functional element and said memory unit constitute a combined unit.

11. (original) The semiconductor device as set forth in Claim 5, wherein said driving unit, said functional element and said memory unit constitute a combined unit.

12. (original) The semiconductor device as set forth in Claim 1, further comprising:

a first signal transferring unit for transferring said data signal to said memory unit from a host device that provides said data signal to the semiconductor device;

a second signal transferring unit for transferring said data signal from said memory unit to said driving unit; wherein

said second signal transferring unit is shorter than said first transferring unit.

13. (original) The semiconductor device as set forth in Claim 4, further comprising:

a first signal transferring unit for transferring said data signal to said memory unit from a host device that provides said data signal to the semiconductor device;

a second signal transferring unit for transferring said data signal from said memory unit to said driving unit; wherein

said second signal transferring unit is shorter than said first transferring unit.

14. (original) The semiconductor device as set forth in Claim 5, further comprising:

a first signal transferring unit for transferring said data signal to said memory unit from a host device that provides said data signal to the semiconductor device;

a second signal transferring unit for transferring said data signal from said memory unit to said driving unit; wherein

said second signal transferring unit is shorter than said first transferring unit.

15. (original) The semiconductor device as set forth in Claim 1, further comprising a level converter for converting an amplitude of said data signal input to said memory unit to a desired amplitude.

16. (original) The semiconductor device as set forth in Claim 4, further comprising a level converter for converting an amplitude of said data signal input to said memory unit to a desired amplitude.

17. (original) The semiconductor device as set forth in Claim 5, further comprising a level converter for converting an amplitude of said data signal input to said memory unit to a desired amplitude.

18. (original) The semiconductor device as set forth in Claim 1, to which a serial signal is to be input, further comprising serial/parallel converter for converting the input serial data signal into a parallel signal.

19. (original) The semiconductor device as set forth in Claim 4, to which a serial signal is to be input, further comprising serial/parallel converter for converting the input serial data signal into a parallel signal.

20. (original) The semiconductor device as set forth in Claim 5, to which a serial signal is to be input, further comprising serial/parallel converter for converting the input serial data signal into a parallel signal.

21. (original) The semiconductor device as set forth in Claim 1, provided with a transference route of an O-phase parallel signal, further comprising:

a phase expanding unit for converting an O-phase parallel signal to a P-phase parallel signal.

22. (original) The semiconductor device as set forth in Claim 4, provided with a transference route of an O-phase parallel signal, further comprising:

a phase expanding unit for converting an O-phase parallel signal to a P-phase parallel signal.

23. (original) The semiconductor device as set forth in Claim 5, provided with a transference route of an O-phase parallel signal, further comprising:

a phase expanding unit for converting an O-phase parallel signal to a P-phase parallel signal.

24. (original) The semiconductor device as set forth in Claim 1, wherein at least one of said driving unit, said first signal transferring unit, said memory unit and said second signal transferring unit is constituted of a thin film transistor.

25. (original) The semiconductor device as set forth in Claim 4, wherein at least one of said driving unit, said first signal transferring unit, said memory unit and said second signal transferring unit is constituted of a thin film transistor.

26. (original) The semiconductor device as set forth in Claim 5, wherein at least one of said driving unit, said first signal transferring unit, said memory unit and said second signal transferring unit is constituted of a thin film transistor.

27. (original) The semiconductor device as set forth in Claim 24, wherein a semiconductor layer of said thin film transistor is constituted of polycrystalline silicon.

28. (original) The semiconductor device as set forth in Claim 25, wherein a semiconductor layer of said thin film transistor is constituted of polycrystalline silicon.

29. (original) The semiconductor device as set forth in Claim 26, wherein a semiconductor layer of said thin film transistor is constituted of polycrystalline silicon.

30-56. (canceled)

57. (original) Driving method of a functional element comprising the steps of:

temporarily storing a data signal for controlling a functional element in a memory unit;

reading out said data signal and transferring said data signal to said functional element; and

transferring said data signal for controlling the functional element from an identical address of said memory unit instead of updating said data signal retained in said memory unit, in case where it is predetermined that the

identical data signal to said data signal stored in said memory unit is to be successively used.

58-61. (canceled)